UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/624,428	LU ET AL.
	Examiner	Art Unit	
	Chikaodili E. Anyikire	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _21 July 2003_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-10_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-10_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _21 July 2003_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _20040408_.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   This application is responsive to application number (10624428) filed on
September 21, 2003. Claims 1-10 are pending and have been examined.

Information Disclosure Statement

2.   Acknowledgement is made of applicant's information disclosure statement.

Drawings

3.   Figures 1 and 2 should be designated by a legend such as --Prior Art-- because

only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in

compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office

action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

4.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
> matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
> conditions and requirements of this title.

5.   Claim 10 rejected under 35 U.S.C. 101 because the claimed invention is directed

to non-statutory subject matter. An acceptable form of the preamble of claim 10, "A

computer readable medium encoded with computer executable instructions for

controlling the processing of a system that decodes a coded data stream, said set of

computer executable instructions performing". See "101 Interim Guidelines for

Examination of Patent Application for Patent Subject Matter Eligibility", Annex IV,

Computer-Related Non-Statutory Subject matter.

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7.   Claim 2 rejected under 35 U.S.C. 102(b) as being anticipated by Yoshioka et al

(US 6,310,921).

As per claim 2, Yoshioka et al disclose a power aware decompression method

for decoding a predicatively encoded data stream, comprising:

(a) generating a first selection signal which signals whether the data to be used

for prediction resides in primary memory in part or in whole (Fig 4; Col 11 Ln 13- Col 11

Ln 28);

(b) if the first selection signal indicates that a portion of the said prediction data or

the whole of the said prediction data is not present in primary memory (Fig 4, 4-6; Col

12 Ln 1-21 and Col 13 Ln 53-Col 14 Ln 9):

i. generating a second selection signal, based on an estimate of the future

needs of the prediction process, to signal that portion of the primary memory

where the prediction data, which is not already present in primary memory,

should reside (Figs 4-6; Col 12 Ln 1-21), and

   ii. transferring said prediction data that is not already present in primary

memory, from secondary memory to that portion of the primary memory indicated

by the second selection signal (Figs 4-6 and 10; Col 11 Ln 13- Ln 41 and Col 12

Ln 1-Col 13 Ln 10), and

   (c) generating a prediction signal to be used in the process of decompression by

manipulating data residing in primary memory (Fig 4-6 and 10; Col 11 Ln 30- Ln 41 and

Col 14 Ln 10-48).

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

9.   The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

   1.   Determining the scope and contents of the prior art.
   2.   Ascertaining the differences between the prior art and the claims at issue.
   3.   Resolving the level of ordinary skill in the pertinent art.
   4.   Considering objective evidence present in the application indicating
         obviousness or nonobviousness.

10.   Claims 1, 3-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Hoogenboom et al (US 5,675,387) in view of Yoshioka et al (US 6,310,921).

        As per claim 1, Hoogenboom et al disclose a decoding power aware encoding

method for generating a predicatively encoded data stream, in which predictions, that

result in a reduction in the amount of data transferred from the secondary memory to

primary memory during the decoding process, are favored, said method for favoring

certain predictions comprising:

        (a) a model (Fig 1) for transfer of data from secondary memory (Fig 1, 22 and 30)

incorporating a memory management in the decoding process (Col 5 Ln 53-61 and Col

6 Ln 56- Col 7 Ln 5);

        (b) a scheme for weighting the relative merits of favoring a certain prediction and

the associated loss in compression gain (Col 11 Ln 35- Col 12 Ln 2), and

        (c) based on said weighting scheme, choosing a particular prediction from the

candidates allowed by the compression scheme (Col 11 Ln 66- Col 12 Ln 2; the prior art

explains the motion vector and the factor being scaled with 2).

        Hoogenboom et al disclose a memory management model that reduces the

number of access to the secondary memory (DRAM 22), which will result in a reduced

power decoding (Col 3 Ln 62-67).

        However, Hoogenboom et al does not explicitly teach using a primary memory in

addition to the secondary memory and conventional buffer memories.

        In the same field of endeavor, Yoshioka et al teach utilizing primary memory (on-

chip memory) in addition to the internal memories as a primary memory (Fig 4, 4).

Therefore, it would have been obvious to one of ordinary skill in the art to have

modified the invention of Hoogenboom et al with the invention of Yoshioka et al to

include the primary memory (on-chip memory) in the memory management system of

Hoogenboom et al. The advantage is the modification allows the invention to reduce

the number of access to the external memory resulting in a decoding system with lower

power consumption.

As per claim 3, Hoogenboom et al disclose a method for decoding a coded data

stream comprising:

(a) processing the coded data stream to produce outputted decoded data frames

(Fig 1, compressed bitstream 4 has been processed to produce output video frames

38);

(b) transmitting signals to and receiving signals from an external memory for

storage and retrieval of previously decoded reference data frames (Fig 1, 22; Col 5 Ln

53- Col 6 Ln 4 and Col 6 Ln 56-59).

(c) transmitting signals to and receiving signals from a memory manager for

retrieval of data frames being decoded currently (fig 1, 30; Col 5 Ln 53-Col 6 Ln 4 and

Col 6 Ln 56-59).

However, Hoogenboom et al does not explicitly teach (c) transmitting signals to

and receiving signals from a primary memory for storage and retrieval of data frames

being decoded currently.

In the same field of endeavor, Yoshioka et al teach (c) transmitting signals to and

receiving signals from a primary memory (Fig 4, 3 and 4) for storage and retrieval of

data frames being decoded currently (Col 12 Ln 8-33 and Col 13 Ln 11-30).

Therefore, it would have been obvious to one of ordinary skill in the art to have

modified the invention of Hoogenboom et al with the invention of Yoshioka et al to

include the primary memory(on-chip memory) in the memory management system of

Hoogenboom et al. The advantage is the modification allows the invention to reduce

the number of access to the external memory resulting in a decoding system with lower

power consumption.

As per claim 4, Hoogenboom et al disclose a system for decoding a coded data

stream comprising:

(a) a processor for outputting the decoded data frames (Fig 1, compressed

bitstream 4 has been processed to produce output video frames 38);

(b) an external memory (Fig 1, 22);

(c) high speed access relative to the external memory's speed (Fig 1, 22 and 30;

Col 6 Ln 15-35 and Col 7 Ln 12-31; DRAM 22 maybe provided as internal memory

within the video decomposition processor), and

(d) a memory management scheme (Fig 1, 30) for decreasing the amount of

traffic to the external memory (Fig 1, 22) so as to provide better real-time performance

and power saving by a connection arrangement for transmission from the processor to

the external memories (Fig 1, 22; Col 3 Ln 39-67).

However, Hoogenboom et al does not explicitly teach an internal primary memory having high speed access relative to the external memory's speed.

In the same field of endeavor, Yoshioka et al teach utilizing an internal memory having high speed access relative to the external memory's speed (Fig 4, 4; Col 12 Ln 8-33 and Col 13 Ln 11-30).

Therefore, it would have been obvious to one of ordinary skill in the art to have modified the invention of Hoogenboom et al with the invention of Yoshioka et al to include the primary memory(on-chip memory) in the memory management system of Hoogenboom et al. The advantage is the modification allows the invention to reduce the number of access to the external memory resulting in a decoding system with lower power consumption.

As per claim 5, Hoogenboom et al disclose a system as defined in claim 4, comprising motion compensation function (Fig 1, 46) of data decoding (Fig 1, 30; Col 6 Ln 36-48).

However, Hoogenboom et al does not explicitly teach said internal primary memory is dedicated to the motion compensation of data decoding.

In the same field of endeavor, Yoshioka et al teach said internal primary memory (Fig 4, 4; Col 12 Ln 8-33 and Col 13 Ln 11-30).

Therefore, it would have been obvious to one of ordinary skill in the art to have modified the invention of Hoogenboom et al with the invention of Yoshioka et al to include the primary memory (on-chip memory) in the memory management system of Hoogenboom et al. The advantage is the modification allows the invention to reduce

the number of access to the external memory resulting in a decoding system with lower

power consumption.

As per claim 6, Hoogenboom et al disclose a system as defined in claim 4,

wherein the processor receives the data stream at its input, and has output respectively

connected to the external memories(Fig 1, 22) and a further output providing decoded

data frames (Fig 1, compressed bitstream 4 has been processed to produce output

video frames 38).

However, Hoogenboom et al does not explicitly teach internal memories.

In the same field of endeavor, Yoshioka et al teach internal memories (Fig 4, 4;

Col 12 Ln 8-33 and Col 13 Ln 11-30).

Therefore, it would have been obvious to one of ordinary skill in the art to have

modified the invention of Hoogenboom et al with the invention of Yoshioka et al to

include the primary memory (on-chip memory) in the memory management system of

Hoogenboom et al. The advantage is the modification allows the invention to reduce

the number of access to the external memory resulting in a decoding system with lower

power consumption.

As per claim 7, Hoogenboom et al disclose a system for decoding a coded data

stream comprising:

(a) a processor for outputting decoded data frames (Fig 1, compressed bitstream

4 has been processed to produce output video frames 38);

(b) motion compensation means having a memory for storing a reference data

frame as well as a data frame being decoded currently (Fig 1, 30 and 46; Col 6 Ln 36-

48);

(c) an external memory (Fig 1, 22; Col 5 Ln 53- Col 6 Ln 48);

(d) high speed access relative to the external memory (Fig 1, 30 and 46; Col 6 Ln

15-35 and Col 7 Ln 12-31; DRAM 22 maybe provided as internal memory within the

video decomposition processor), and

(e) motion compensation function of decoding (Fig 1, 30, 42, 44, and 46; Col 6

Ln 36-48).

However, Hoogenboom et al does not explicitly teach an internal memory having

high speed access relative to the external memory.

In the same field of endeavor, Yoshioka et al teach an internal memory having

high speed access relative to the external memory (Fig 4, 4; Col 12 Ln 8-33 and Col 13

Ln 11-30).

Therefore, it would have been obvious to one of ordinary skill in the art to have

modified the invention of Hoogenboom et al with the invention of Yoshioka et al to

include the primary memory (on-chip memory) in the memory management system of

Hoogenboom et al. The advantage is the modification allows the invention to reduce

the number of access to the external memory resulting in a decoding system with lower

power consumption.

As per claim 10, arguments analogous to those presented for the rejection of

claim 3 are applicable to the rejection claim 10.

Furthermore, Yoshioka's memory controller 6 (Figs 4 and 10) controls the

amount of traffic to the external memory.

11.   Claims 8 and 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee

et al (US 5,675,387) in view of Yoshioka et al (US 6,310,921).

As per claim 8, Lee et al disclose a system for encoding an input data frame

comprising:

(a) a motion estimator for receiving an input frame and for searching to find the

best match between an input frame and an area in a reference frame (Fig 1, 20; Col 4

Ln 1-9 and Col 4 Ln 64- Col 5 Ln 7);

(c) a motion vector selector coupled to the output of the motion estimator (Fig 8,

106, 108, and 110; Col 9 Ln 59- Col 10 Ln 65);

(d) a memory for storing data reference frames (Fig 1, 16; Col 4 Ln 48-63), and

(e) a quality and rate controller coupled to the motion vector selector (Fig 8, 100,

102, 104; Col 9 Ln 59- Col 10-65).

However, Lee et al does not explicitly teach a primary memory model coupled to

the motion estimator.

In the same field of endeavor, Yoshioka et al teach a primary memory model (Fig

4, 4) coupled to the motion estimator (Fig 4, 7; Col 13 Ln 11-30).

Therefore, it would have been obvious to one of ordinary skill in the art to have

modified the invention of Lee et al with the invention of Yoshioka et al to include the

primary memory (on-chip memory) in the memory management system of Hoogenboom

et al. The advantage is the modification allows the invention to reduce the number of access to the external memory resulting in a decoding system with lower power consumption.

As per claim 9, Lee et al disclose a system for encoding a data frame as defined in claim 8 further comprising a motion vectors module for determining the motion vectors based on the current block and the best matched candidate (Fig 7; Col 8 Ln 7-67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chikaodili E. Anyikire whose telephone number is (571) 270-1445. The examiner can normally be reached on Monday to Friday, 7:30 am to 5 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571) 272 - 7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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